THE AMENDMENTS

In The Claims

1. (Currently Amended) A processor readable medium encoding a data structure for supporting one or more packet modification operations, the data structure comprising:

a first pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area; and

a second pointer to a burst of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

wherein the data structure is located in a third memory and the data structure is accessed via a data structure index, wherein the data structure index is embedded in the one or more packets;

wherein data is selectively shifted and masked in each of plurality of categories responsive to the one or more decoded commands, thereby performing one or more packet modification operations in the packet;

wherein the selectively shifted and masked data is logically summed into the plurality of categories.

2. (Currently Amended) The processor readable medium of claim 1 wherein the ~~first and second memory areas are located in different memories~~ data structure is generated during receive-side classifications processing of a packet.

3. (Currently Amended) The processor readable medium of claim 1 wherein the ~~first and second memory areas are located in the same memory~~ data structure is generated by a host CPU coupled to a switch fabric.

4. (Original) The processor readable medium of claim 1 wherein the one or more commands are stored in a packed format.

5. (Original) The processor readable medium of claim 1 wherein the one or more data or mask items are stored in a packed format.

6. (Original) The processor readable medium of claim 1 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip from a modification processor configured to execute the one or more commands.

8. (Original) The processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip with the modification processor.

9. (Original) The processor readable medium of claim 1 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

10. (Original) The processor readable medium of claim 9 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.

11. (Currently Amended) A method of performing one or more packet modification operations on a packet ~~while located within a first portion of a switch, the packet including a data structure index previously added while the packet was located within a second portion of the switch~~, the method comprising:

performing packet classification while the packet is located within a first portion of a switch;

inserting a data structure index in the packet while the packet is located within a second portion of the switch;

retrieving from a memory a data structure corresponding to the data structure index, and comprising first a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area, and a second pointer to a burst of one or more data or mask

items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

retrieving from the first memory area the one or more commands;

retrieving from the second memory area the one or more data or mask items for use by the one or more commands; and

executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet;

wherein the data structure is located in a third memory and the data structure is accessed via a data structure index, wherein the data structure index is embedded in the one or more packets;

wherein data is selectively shifted and masked in each of plurality of categories responsive to the one or more decoded commands, thereby performing one or more packet modification operations in the packet;

wherein the selectively shifted and masked data is logically summed into the plurality of categories.

12. (Original) The method of claim 11 wherein the first portion of the switch is an egress portion of the switch.

13. (Original) The method of claim 11 wherein the second portion of the switch is an ingress portion of the switch.

14. (Currently Amended) The method of claim 12 wherein the ~~first and second memory areas are located in different memories~~ data structure is generated during receive-side classifications processing of a packet.

15. (Currently Amended) The method of claim 12 wherein the ~~first and second memory areas are located in the same memory~~ data structure is generated by a host CPU coupled to a switch fabric.

16. (Original) The method of claim 12 wherein the one or more commands are stored in a packed format.

17. (Original) The method of claim 12 wherein the one or more data or mask items are stored in a packed format.

18. (Original) The method of claim 12 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19. (Original) The method of claim 12 wherein the first and second memory areas are located in a memory implemented off chip from a modification processor which executes the one or more commands.

20. (Original) The method of claim 12 wherein the first memory area is located in a memory implemented on chip with the modification processor.

21. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

22. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.

23. (Canceled)

24. (New) A pipeline processor core comprising:

a data structure comprising two or more pointers;

a command fetch stage configured to fetch one or more commands obtained using a first pointer to access a first memory;

a command decode stage configured to decode the one or more commands;

an address and mask generation stage configured to generate one or more addresses and one or more mask for each of the commands;

a data shift, mask and sum stage wherein packet data is selectively shifted and masked in each of plurality of categories in response to a decoded command, wherein data shifting and masking is based upon a burst of one or more data and mask items obtained using a second pointer to access a second memory which is distinct from the

first memory;

wherein the pipeline processor core supports a data structure comprising two or more pointers;

wherein the first and second pointers are located in the data structure that is accessed from a third memory via a data structure index, wherein the data structure index is embedded in one or more data packets;

wherein the selectively shifted and masked data is logically summed into the plurality of categories.

25. (New) The processor readable medium of claim 1 wherein the plurality of categories comprises packet data, insertion or replacement data, copy data, and residual packet data.

26. (New) The processor readable medium of claim 25 wherein the plurality of categories supports a nested packet format.

27. (New) The pipeline processor core of claim 24 wherein a transmit modification index is coupled to the data shift, mask and sum stage.